AMENDMENTS TO THE CLAIMS

Amend the claims as follows. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently amended) A circuit for controlling a ~~the~~ duty cycle and jitter of a clock signal, comprising:

an input node for receiving the clock signal;

a plurality of serially connected delay elements coupled to the input node, said plurality of delay elements creating a delayed clock signal;

a phase detector having a first input coupled to said clock signal and a second input coupled to an output of said plurality of delay elements for receiving a delayed clock signal therefrom, said phase detector operating so as to generate an error signal that is indicative of a phase difference between said clock signal and said delayed clock signal, said error signal being coupled to at least a first one of said delay elements for controlling said at least one delay element for minimizing the phase difference between said clock signal and said delayed clock signal;

a first divider circuit having an input coupled to said clock signal;

a second divider circuit having an input coupled to an output of said first one of said plurality of delay elements for receiving the delayed clock signal therefrom;

a gate having inputs coupled to outputs of said first and second divider circuits and an output; and

an output node coupled to the output of the gate for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is ~~varied~~ controlled so as to provide a predetermined processed clock signal duty cycle.

2. (Original) A circuit as in claim 1, wherein said predetermined duty cycle is a nominally 50-50 duty cycle.

3. (Original) A circuit as in claim 1, wherein said output node is coupled to baseband circuitry of a wireless communications terminal.

4. (Cancelled)

5. (Currently amended) A method ~~for processing a clock signal,~~ comprising:

~~providing a clock control circuit having an input node and an output node;~~

receiving ~~the~~ a clock signal ~~at the input node~~;

generating a delayed clock signal;

generating an error signal that is indicative of a phase difference between the clock signal and the delayed clock signal;

minimizing the phase difference between the clock signal and the delayed clock signal in accordance with the error signal;

dividing both the clock signal and the delayed clock signal, creating a modified clock signal and a modified delayed clock signal; and

performing an exclusive or operation between the modified clock signal and modified delayed clock signal ~~and outputting~~ to create a processed clock signal ~~from the output node~~, the processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is ~~varied~~ controlled so as to provide a predetermined processed clock signal duty cycle.

6. (Original) A method as in claim 5, wherein the predetermined duty cycle is a 50-50 duty cycle.

7. (Currently amended) A method as in claim 5, ~~wherein the output node is coupled~~ further comprising coupling the processed clock signal to baseband circuitry of a wireless communications terminal.

8. (Original) A method as in claim 5, wherein the first edge of the processed clock signal is a rising edge that is synchronized to a rising edge of the clock signal.

9. (New) A method as in claim 5 wherein the first edge of the processed clock signal is relatively jitter free in comparison to the second edge of the processed clock signal.

10. (New) A circuit comprising:

an input configured to receive a clock signal;

delay elements coupled to the input, the delay elements configured to generate a delayed clock signal;

a phase detector coupled to the input and to the delay elements, the phase detector configured to generate an error signal that is indicative of a phase difference between the clock signal and the delayed clock signal;

the delay elements coupled to the phase detector, the delay elements further configured to minimize the phase difference between the clock signal and the delayed clock signal in accordance with the error signal;

dividing elements coupled to the input and to the delay elements, the dividing elements configured to divide both the clock signal and the delayed clock signal to create a modified clock signal and a modified delayed clock signal;

an exclusive or element coupled to the dividing elements, the exclusive or element configured to perform an exclusive or operation between the modified clock signal and modified delayed clock signal, the exclusive or element creating a processed clock signal, the processed clock signal having a first edge that is synchronized to an

edge of the clock signal and a second edge that is controlled so as to provide a predetermined processed clock signal duty cycle; and

an output configured to output the processed clock signal, the output coupled to the exclusive or element.

11. (New) A circuit as in claim 10 wherein the first edge of the processed clock signal is relatively jitter free in comparison to the second edge of the processed clock signal.